UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/497,533	02/03/2000	Samuel D. Naffziger	10990471-1	7597

22879 7590 07/15/2003

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER
HARKNESS, CHARLES A

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 07/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/497,533	Applicant(s) NAFFZIGER, SAMUEL D.
	Examiner Charles A Harkness	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. In view of Applicant's amendment to the claims, the previous objection to the claims has been withdrawn.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-23 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The independent claims have the limitations of "each said instruction port having a respective self-timed vector logic element" which is not supported in the specification. Applicant's specification discloses using a clock signal in both the specification (page 9 line 5) and in the figures (Figure 3A under "PRCHRG" in parentheses is E.G.CLK), thus teaching away from being self-timed, and gives no other support for such a claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-23 are rejected under 35 U.S.C. 102(b) as being anticipated by Lesartre et. al., U.S. Patent Number 5,761,474 (herein referred to as Lesartre).

5. Referring to claim 1 Lesartre has taught a method for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in an instruction reordering mechanism of a processor that can execution of instructions out of order via a predefined number of ports (Lesartre column 6 lines 57-63; since in Lesartre's preferred embodiment, there are 4 ports to the execution units open per cycle, 2 for integer and 2 for floating-point, no more than 4 instructions could be allowed to launch per cycle), comprising the steps of:

(a) providing said instruction reordering mechanism having a plurality of said instructions, each said instruction port having respective logic element for causing and preventing launching, when appropriate, of said instruction (Lesartre column 2 lines 23-28 and 42-47); and

(b) propagating a set of signals successively during a launch cycle through said logic elements of said instruction reordering mechanism (Lesartre column 2 lines 27-42 and 60-66; and column 7 lines 29-31 ; and column 1 lines 10-12, plurality of instructions interpreted as issuing one instruction after another and so on; the system taught by Lesartre would propagate the signals during a launch cycle so that the system knew which instructions to launch. If the signals were propagated after the launch cycle, the system would not be able to properly function; inherently, the system would have to keep track of which ports are available; otherwise the system may try to launch two slots using the same port, which what cause an error; only one slot can be launched in each port, so it is required of the system to track which port is or is not available for each clock cycle).

6. Referring to claim 2 Lesartre has taught where the method further comprises the step of advising each instruction of said instruction port reordering mechanism during each launch cycle either that said instruction will be launched or that said instruction will not be launched (Lesartre column 2 line 60-column 3 line 8 and column 2 lines 36-42).

7. Referring to claim 3 Lesartre has taught wherein said signals are propagated through said logic elements in response to only one direction of logic transition (Lesartre column 2 lines 36-42 and column 2 line 60-column 3 line 8; and as shown in figure 4, the valop signal, 151, only propagates in one direction).

8. Referring to claim 4 Lesartre has taught where the method further comprises the step of communicating said predefined plurality of said instructions to a corresponding predefined plurality of ports associated with one or more execution resources (Lesartre column 5 lines 26-30 and 41-46).

9. Referring to claim 5 Lesartre has taught where the method further comprises the step of, after said predefined plurality of said instructions have been selected, propagating a lost signal to remaining logic elements associated with remaining instructions of said instruction reordering mechanism to indicate to said remaining logic elements that their respective remaining instructions have not been selected (Lesartre column 2 lines 35-48; valop signal is propagated forward between the aslots showing if there is a dependency precedes, and if so, indicating to the other aslots that they have not been selected).

10. Referring to claim 6 Lesartre has taught where the method further comprises the of steps:

(c) after said predefined plurality of said instructions have been selected, propagating a lost signal to remaining logic elements associated with remaining instructions of said instruction

reordering mechanism to indicate to said remaining logic elements that their respective remaining instructions have not been selected (Lesartre column 2 lines 35-48; valop signal is propagated forward between the aslots showing if there is a dependency precedes, and if so, indicating to the other aslots that they have not been selected);

(d) performing steps (b) and (c) during a single cycle associated with one or more execution resources (Lesartre column 2 lines 35-42, the valop signal is used for rejecting both steps (b) and (c), therefore the steps must occur in a single cycle, because it is the same signal); and

(e) communicating said predefined plurality of said instructions from said instruction reordering mechanism to a corresponding predefined plurality of ports associated with said one or more execution resources (Lesartre column 5 lines 26-30 and 41-46).

11. Referring to claim 7 Lesartre has taught where the method further comprises the of steps:

(c) providing said instruction reordering mechanism in a form of a queue having a plurality of slots, each said slot having a respective one of said logic elements and means for temporarily storing a respective instruction (Lesartre column 2 lines 18-28 and column 5 lines 26-30); and

(d) propagating said set of said signals successively through said slots of said queue during an execution cycle (Lesartre column 2 lines 36-42 and column 2 line 60-column 3 line 8).

12. Referring to claim 8 Lesartre has taught wherein said set comprises two of more signals (Lesartre column 2 lines 36-42 and column 2 line 60-column 3 line 8).

13. Referring to claim 9 Lesartre has taught where the method further comprises of step:

(c) causing said propagation through only a predefined number of said logic elements during a launch cycle (Lesartre column 12 lines 41-42).

14. Referring to claim 10 Lesartre has taught a method for quickly finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in a queue of a processor that can launch execution of instructions out of order, so that the found instructions can be communicated to a corresponding predefined plurality of ports associated with one or more execution resources, comprising the steps of:

(a) providing said queue having a plurality of slots, each said slot for temporarily storing a respective instruction and launching, when appropriate, execution of said respective instruction (Lesartre column 2 lines 18-28 and column 5 lines 26-30, plurality of instructions interpreted as issuing one instruction after another and so on); and

(b) propagating a set of signals successively through slots of said queue during a launch cycle that, when passed through a particular slot:

(1) selects said particular slot for launching when said particular slot is ready by asserting in said slot one or more found signals that identify one or more specific ports associated with said one or more execution resources (Lesartre column 7 lines 24-31);

(2) refrains from selecting said particular slot when said particular slot is not ready by asserting in said slot a lost signal (Lesartre column 2 lines 35-48; valop signal is propagated forward between the aslots showing if there is a dependency precedes, and if so, indicating to the other aslots that they have not been selected);

(3) keeps track of how many slots have been selected during said launch cycle (Lesartre column 10 lines 50-57, since the signal keeps track if a producer instruction as being present or not, it keeps track of how many slots have been selected); and

(4) causes selection of no more than said predefined plurality of said instructions during said launch cycle; and wherein propagating occurs in response to logic transitions in only one direction (Lesartre column 10 lines 37-49, once the asserted valop signal is propagated to the other slots, it will prevent anymore slots from being selected once a dependency is found; and as shown in figure 4, the valop signal, 151, only propagates in one direction).

15. Referring to claim 11 Lesartre has taught where the method further comprises of the step of communicating said predefined plurality of said instructions from said queue to said corresponding predefined plurality of ports associated with said one or more execution resources (Lesartre column 5 lines 26-30 and 41-46).

16. Referring to claim 12 Lesartre has taught where the method further comprises of the step of:

(c) during said launch cycle but after said predefined plurality of said instructions have been selected, propagating a lost signal to remaining slots associated with remaining instructions of said queue to indicate to said remaining slots that their respective remaining instructions have not been selected (Lesartre column 2 lines 35-48; valop signal is propagated forward between the aslots showing if there is a dependency precedes, and if so, indicating to the other aslots that they have not been selected).

17. Referring to claim 13 Lesartre has taught a system for finding a predefined plurality of instructions, if available, that are ready to be executed in a processor that can launch execution of instructions out of order, comprising:

(a) an instruction reordering mechanism for temporarily storing a plurality of said instructions (Lesartre column 2 lines 15-25, plurality of instructions interpreted as issuing one instruction after another and so on); and

(b) a plurality of logic elements associated with said instruction reordering mechanism and associated respectively with each of said instructions in said instruction reordering mechanism for causing and preventing launching, when appropriate, of respective instructions, said logic elements configured to propagate a plurality of signals through said logic elements such that causes said logic elements to select said predefined plurality of said instructions for launching and to de-select any remaining instructions in response to only one direction of logic transition (Lesartre column 2 lines 23-47; the system taught by Lesartre would propagate the signals during a launch cycle so that the system knew which instructions to launch. If the signals were propagated after the launch cycle, the system would not be able to properly function; and as shown in figure 4, the valop signal, 151, only propagates in one direction).

18. Referring to claim 14 Lesartre has taught wherein each one of said logic elements is configured to receive said set of signals from a previous logic element, to evaluate said set of signals to determine whether or not to launch a respective instruction, to modify states associated with said set of signals based upon whether or not said respective instruction was launched, and to propagate said set of said signals to a later logic element (Lesartre column 2 lines 36-56 and lines 60-66 and column 7 lines 24-26).

19. Referring to claim 15 Lesartre has taught wherein each of said logic elements is implemented in combination logic hardware (Lesartre column 3 lines 28-32 and column 2 lines 25-29, where a latch is known to be combinational logic).

20. Referring to claim 16 Lesartre has taught wherein each said logic element is configured to, after said predefined plurality of said instructions have been selected, propagate a lost signal to remaining logic elements associated with said remaining instructions of said instruction reordering mechanism to indicate to said remaining logic elements that their respective remaining instructions have not been selected (Lesartre column 2 lines 35-48; valop signal is propagated forward between the aslots showing if there is a dependency precedes, and if so, indicating to the other aslots that they have not been selected).

21. Referring to claim 17 Lesartre has taught that the system further comprises of one or more execution resources having one of more ports to receive data from said predefined plurality of said instructions (Lesartre column 5 lines 26-30 and 41-46).

22. Referring to claim 18 Lesartre has taught wherein at least one of said execution resources is an arithmetic logic unit (ALU) (Lesartre figure 3 reference number 42' and column 5 lines 11-15).

23. Referring to claim 19 Lesartre has taught wherein at least one of said execution resources is a multiple accumulate unit (MAC) (Lesartre figure 3 reference number 42'' and column 5 lines 15-22).

24. Referring to claim 20 Lesartre has taught wherein at least one of said execution resources is a cache (Lesartre figure 1 reference number 24 and column 4 lines 55-60).

25. Referring to claim 21 Lesartre has taught wherein said instruction reordering mechanism is a queue (Lesartre column 2 lines 15-22).

26. Referring to claim 22 Lesartre has taught a system further comprising of an arbitration mechanism configured to assert a start signal to one of said logic elements to initiate said propagation of said set of signals (Lesartre column 8 lines 16-25).

27. Referring to claim 23 Lesartre has taught a system for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in a queue of a processor that can launch execution of instructions out of order, comprising:

(a) queue means for storing a plurality of said instructions, said queue means having a plurality of launch logic means for causing and preventing launching, when appropriate, of a respective instruction (Lesartre column 2 lines 15-32 and lines 42-48, plurality of instructions interpreted as issuing one instruction after another and so on); and

(b) logic means associated with said queue, said logic means for propagating a set of signals to successive launch logic means to indicate both when and which of one or more ports of one or more execution resources are available for each said instruction and when none of said ports are available, wherein said means for propagating is responsive to logic transitions in only one direction (Lesartre column 10 line 50-column 11 line 8, since the valop signal indicates whether there is a producer instruction, or an instruction being sent to the execution unit, the signal indicates whether a execution unit is available or not; and as shown in figure 4, the valop signal, 151, only propagates in one direction).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

28. Claims 1-9 and 13-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lesartre in view of Microsoft Computer Dictionary, 4th Edition (herein referred to as MCD).

29. Referring to claim 1 Lesartre has taught a method for finding a predefined plurality of instructions, if available, that are ready to be executed and that reside in an instruction reordering mechanism of a processor that can execution of instructions out of order via a predefined number of ports (Lesartre column 6 lines 57-63; since in Lesartre's preferred embodiment, there are 4 ports to the execution units open per cycle, 2 for integer and 2 for floating-point, no more than 4 instructions could be allowed to launch per cycle), comprising the steps of:

(a) providing said instruction reordering mechanism having a plurality of said instructions, each said instruction port having respective logic element for causing and preventing launching, when appropriate, of said instruction (Lesartre column 2 lines 23-28 and 42-47); and

(b) propagating a set of signals successively during a launch cycle through said logic elements of said instruction reordering mechanism (Lesartre column 2 lines 27-42 and 60-66; and column 7 lines 29-31 ; and column 1 lines 10-12, plurality of instructions interpreted as issuing one instruction after another and so on; the system taught by Lesartre would propagate the signals during a launch cycle so that the system knew which instructions to launch. If the signals were propagated after the launch cycle, the system would not be able to properly

function; inherently, the system would have to keep track of which ports are available; otherwise the system may try to launch two slots using the same port, which what cause an error; only one slot can be launched in each port, so it is required of the system to track which port is or is not available for each clock cycle).

Lesartre has not taught having a self-timed vector logic unit. MCD has taught asynchronous communications can start and stop at any time instead of having to match the timing governed by a clock (MCD page 32, definition of asynchronous). One of ordinary skill in the art at the time of the invention would have recognized after looking at both Lesartre and MCD that by issuing instructions when they are available, and not waiting for a clock signal or some other indicator signal, they can begin execution on the instructions earlier, and thus reducing the amount of time required to execute a program. If each logic unit had to wait for a clock pulse, or some other propagating signal to indicate when it could issue an instruction, it would simply wait for the signal and do nothing till it received such a signal, and be wasting time. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of MCD with the system of Lesartre to have the vector logic units self-timed to reduce the time required for execution.

30. Referring to claim 2 Lesartre has taught where the method further comprises the step of advising each instruction of said instruction port reordering mechanism during each launch cycle either that said instruction will be launched or that said instruction will not be launched (Lesartre column 2 line 60-column 3 line 8 and column 2 lines 36-42).

31. Referring to claim 3 Lesartre has taught wherein said signals are propagated through said logic elements in response to only one direction of logic transition (Lesartre column 2 lines 36-

42 and column 2 line 60-column 3 line 8; and as shown in figure 4, the valop signal, 151, only propagates in one direction).

32. Referring to claim 4 Lesartre has taught where the method further comprises the step of communicating said predefined plurality of said instructions to a corresponding predefined plurality of ports associated with one or more execution resources (Lesartre column 5 lines 26-30 and 41-46).

33. Referring to claim 5 Lesartre has taught where the method further comprises the step of, after said predefined plurality of said instructions have been selected, propagating a lost signal to remaining logic elements associated with remaining instructions of said instruction reordering mechanism to indicate to said remaining logic elements that their respective remaining instructions have not been selected (Lesartre column 2 lines 35-48; valop signal is propagated forward between the aslots showing if there is a dependency precedes, and if so, indicating to the other aslots that they have not been selected).

34. Referring to claim 6 Lesartre has taught where the method further comprises the of steps:

(c) after said predefined plurality of said instructions have been selected, propagating a lost signal to remaining logic elements associated with remaining instructions of said instruction reordering mechanism to indicate to said remaining logic elements that their respective remaining instructions have not been selected (Lesartre column 2 lines 35-48; valop signal is propagated forward between the aslots showing if there is a dependency precedes, and if so, indicating to the other aslots that they have not been selected);

(d) performing steps (b) and (c) during a single cycle associated with one or more execution resources (Lesartre column 2 lines 35-42, the valop signal is used for rejecting both

steps (b) and (c), therefore the steps must occur in a single cycle, because it is the same signal); and

(e) communicating said predefined plurality of said instructions from said instruction reordering mechanism to a corresponding predefined plurality of ports associated with said one or more execution resources (Lesartre column 5 lines 26-30 and 41-46).

35. Referring to claim 7 Lesartre has taught where the method further comprises the of steps:

(c) providing said instruction reordering mechanism in a form of a queue having a plurality of slots, each said slot having a respective one of said logic elements and means for temporarily storing a respective instruction (Lesartre column 2 lines 18-28 and column 5 lines 26-30); and

(d) propagating said set of said signals successively through said slots of said queue during an execution cycle (Lesartre column 2 lines 36-42 and column 2 line 60-column 3 line 8).

36. Referring to claim 8 Lesartre has taught wherein said set comprises two of more signals (Lesartre column 2 lines 36-42 and column 2 line 60-column 3 line 8).

37. Referring to claim 9 Lesartre has taught where the method further comprises of step:

(c) causing said propagation through only a predefined number of said logic elements during a launch cycle (Lesartre column 12 lines 41-42).

38. Referring to claim 13 Lesartre has taught a system for finding a predefined plurality of instructions, if available, that are ready to be executed in a processor that can launch execution of instructions out of order, comprising:

(a) an instruction reordering mechanism for temporarily storing a plurality of said instructions (Lesartre column 2 lines 15-25, plurality of instructions interpreted as issuing one instruction after another and so on); and

(b) a plurality of logic elements associated with said instruction reordering mechanism and associated respectively with each of said instructions in said instruction reordering mechanism for causing and preventing launching, when appropriate, of respective instructions, said logic elements configured to propagate a plurality of signals through said logic elements such that causes said logic elements to select said predefined plurality of said instructions for launching and to de-select any remaining instructions in response to only one direction of logic transition (Lesartre column 2 lines 23-47; the system taught by Lesartre would propagate the signals during a launch cycle so that the system knew which instructions to launch. If the signals were propagated after the launch cycle, the system would not be able to properly function; and as shown in figure 4, the valop signal, 151, only propagates in one direction).

Lesartre has not taught having a self-timed vector logic unit. MCD has taught asynchronous communications can start and stop at any time instead of having to match the timing governed by a clock (MCD page 32, definition of asynchronous). One of ordinary skill in the art at the time of the invention would have recognized after looking at both Lesartre and MCD that by issuing instructions when they are available, and not waiting for a clock signal or some other indicator signal, they can begin execution on the instructions earlier, and thus reducing the amount of time required to execute a program. If each logic unit had to wait for a clock pulse, or some other propagating signal to indicate when it could issue an instruction, it would simply wait for the signal and do nothing till it received such a signal, and be wasting

time. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of MCD with the system of Lesartre to have the vector logic units self-timed to reduce the time required for execution.

39. Referring to claim 14 Lesartre has taught wherein each one of said logic elements is configured to receive said set of signals from a previous logic element, to evaluate said set of signals to determine whether or not to launch a respective instruction, to modify states associated with said set of signals based upon whether or not said respective instruction was launched, and to propagate said set of said signals to a later logic element (Lesartre column 2 lines 36-56 and lines 60-66 and column 7 lines 24-26).

40. Referring to claim 15 Lesartre has taught wherein each of said logic elements is implemented in combination logic hardware (Lesartre column 3 lines 28-32 and column 2 lines 25-29, where a latch is known to be combinational logic).

41. Referring to claim 16 Lesartre has taught wherein each said logic element is configured to, after said predefined plurality of said instructions have been selected, propagate a lost signal to remaining logic elements associated with said remaining instructions of said instruction reordering mechanism to indicate to said remaining logic elements that their respective remaining instructions have not been selected (Lesartre column 2 lines 35-48; valop signal is propagated forward between the aslots showing if there is a dependency precedes, and if so, indicating to the other aslots that they have not been selected).

42. Referring to claim 17 Lesartre has taught that the system further comprises of one or more execution resources having one of more ports to receive data from said predefined plurality of said instructions (Lesartre column 5 lines 26-30 and 41-46).

43. Referring to claim 18 Lesartre has taught wherein at least one of said execution resources is an arithmetic logic unit (ALU) (Lesartre figure 3 reference number 42' and column 5 lines 11-15).

44. Referring to claim 19 Lesartre has taught wherein at least one of said execution resources is a multiple accumulate unit (MAC) (Lesartre figure 3 reference number 42'' and column 5 lines 15-22).

45. Referring to claim 20 Lesartre has taught wherein at least one of said execution resources is a cache (Lesartre figure 1 reference number 24 and column 4 lines 55-60).

46. Referring to claim 21 Lesartre has taught wherein said instruction reordering mechanism is a queue (Lesartre column 2 lines 15-22).

47. Referring to claim 22 Lesartre has taught a system further comprising of an arbitration mechanism configured to assert a start signal to one of said logic elements to initiate said propagation of said set of signals (Lesartre column 8 lines 16-25).

Response to Arguments

48. Applicant's arguments filed 06/30/03, paper number 9, have been fully considered but they are not persuasive.

49. In the remarks, in regard to the rejection of claim 1 on page 11 and the rejection of claim 13 on pages 13-14, Applicant argues in essence that:

"Specifically, the '474 patent fails to disclose, teach, or suggest, "each said instruction port having a respective self-timed vector logic element."

50. This is not found persuasive, since there is no support for the claim amendment, as indicated in the 112 rejection of the claims listed above. Applicant's specification discloses using

a clock signal in both the specification (page 9 line 5) and in the figures (Figure 3A under "PRCHRG" in parentheses is E.G.CLK), thus teaching away from being self-timed, and gives no other support for such a claim.

51. In the remarks, in regard to the rejection of claim 10 on page 12 and the rejection of claim 23 on page 15, Applicant argues in essence that:

"Specifically, the '474 patent fails to disclose, teach, or suggest Applicant's claimed step of 'propagating a set of signals successively through slots of said queue during a launch cycle...wherein propagating occurs in response to logic transitions in only one direction.' In this regard, the '474 patent apparently describes circuit embodiments responsive to clock signals. That is, clock signals direct the propagation of operand dependency logic."

52. This is not found persuasive. Lesartre has taught wherein the propagating only occurs in logic transitions in one direction as shown in figure 4, the valop signal, 151, only propagates in one direction, as indicated by the direction arrow (Lesartre column 7 line 64-column 8 line 4 also indicates that the valop signal, 151, is only propagated in a single direction). Also, there is no reason given as why Lesartre using a clock signal to direct the propagation of operand dependency logic does not read on the claims. The clock does not switch the direction of the signal, but simply is the control for when the signal is propagated. Refer back to the previous argument and the 112 rejection listed above. There is nothing in claims 10 or 23 that limit them from using a clock from being used to control a set of propagating signals.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Charles A Harkness whose telephone number is 703-305-7579. The examiner can normally be reached on 8:00 A.M. – 5:30 P.M. with every other Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 703-305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-7579.

Charles Allen Harkness

Examiner

Art Unit 2183

July 11, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100